CLAIMS

What is claimed is:

1. A layout comprising for an even number of discrete transistors, N, comprising:

a first half of the transistors (N/2) oriented along a first axis,

a second half of the transistors (N/2) oriented along a second axis orthogonal to the first half of the transistors.

2. The layout of claim 1, wherein the transistor layout is bilaterally symmetric along both the X and Y axis.

3. The layout of claim 1, comprising:

a plurality of legs arranged in a bilaterally symmetric format, the legs forming the gates of the N transistors.

4. The layout of claim 3, further comprising:

diffused areas forming sources and drains; and

an area at which any of the plurality of legs cross, the area being a non-diffused area.

5. The layout of claim 3, wherein the plurality of legs form a tic-tac-toe pattern.

6. The layout of claim 5, wherein

the tic-tac-toe pattern defines square areas between the legs; and

the source and drain areas alternate in the square areas.

7. The layout of claim 5, wherein the tic-tac-toe pattern may be repeated to form a larger layout.

8. The layout of claim 1, used for an integrated circuit, wherein the gate orientation reduces skew effects due to mask alignment and gate orientation.

9. A symmetric transistor layout comprising:

an even number of transistor legs, laid out in an intersecting pattern, forming a bilaterally symmetric base;

a plurality of source areas and drain areas defined by rectangles enclosed by two or more transistor legs; and

undiffused areas defined by an intersection of the legs;

a plurality of transistors defined by a portion of a leg forming a gate and the source and drain areas on either side of the leg forming a source and a drain.

10. The symmetric transistor layout of claim 9, wherein the plurality of transistors is an even number of transistors.

11. The symmetric transistor layout of claim 10, wherein a first half of the transistors are horizontally oriented and a second half of the transistors are vertically oriented.

12. The symmetric transistor layout of claim 9, wherein the plurality of legs form a tic-tac-toe pattern.

13. A method of making a symmetric transistor device comprising:

depositing a first conductive layer on a substrate, the first conductive layer forming an even number of transistor legs, laid out in an intersecting pattern, forming a bilaterally symmetric base;

doping the substrate to form source and drain regions; and

forming a plurality of transistors defined by a portion of a leg forming a gate and the source and drain areas on either side of the leg forming a source and a drain.

14. The method of claim 13, further comprising:

depositing a silicon dioxide prior to depositing the first conductive layer.

15. The method of claim 13, wherein a diffusion plate used for doping forms undoped areas at intersections of the transistor legs.

16. The method of claim 13, wherein the intersecting pattern forms a tic-tac-toe pattern.

17. The method of claim 13, wherein the first conductive layer comprises polysilicon.

18. The method of claim 13, further comprising:

conductive interconnections between the source and drain areas to form a circuit.

19. The method of claim 13, wherein a first half of the transistors are oriented along a first axis and a second half of the transistors (N/2) oriented along a second axis orthogonal to the first half of the transistors.

20. The method of claim 19, wherein the minimum drawn W/L is used for each transistor leg.